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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

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INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP98/00963	March 9, 1998	Japanese Patent Application No. 9-142575 filed on May 30, 1997

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND DRIVING METHOD THEREOF

APPLICANT(S) FOR DO/EO/US: Akihide SHIBATA and Hiroshi IWATA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. § 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. § 371.
3. ☐ This express request to begin national examination procedures (35 U.S.C. § 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. § 371(b) and PCT Articles 22 and 39(1).
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. § 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. § 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. § 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. § 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. § 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. § 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. §§ 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. §§ 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: Return receipt postcard.

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Gary Paul Lazzo

pa-433254

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U.S. APPLICATION NO. (If known, see 37 C.F.R. §1.5) To Be Assigned 09/424966	INTERNATIONAL APPLICATION NO. PCT/JP98/00963	DOCKET NUMBER: 247322001700

17.* ☐ The following fees are submitted:

BASIC NATIONAL FEE (37 C.F.R. §§ 1.492(a)(1)-(5)):

	CALCULATIONS PTO USE ONLY
Search Report has been prepared by the EPO or JPO $840.00	
International preliminary examination fee paid to (USPTO (37 C.F.R. § 1.482)..... $670.00	
No international preliminary examination fee paid to USPTO (37 C.F.R. § 1.482) but international search fee paid to USPTO (37 C.F.R. § 1.445(a)(2))..... $760.00	
Neither international preliminary examination fee (37 C.F.R. § 1.482) nor international search fee (37 C.F.R. § 1.445(a)(2)) paid to USPTO $970.00	
International preliminary examination fee paid to USPTO (37 C.F.R. § 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4)..... $96.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$970.00
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. § 1.492(e)).	$

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$*
Total claims	45 - 20 =	25	x $18.00	$ 450.00
Independent claims	4 - 3 =	1	x $78.00	$ 78.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $260.00	$ 260.00
TOTAL OF ABOVE CALCULATIONS =				$ 788.00
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 C.F.R. §§ 1.9, 1.27, 1.28)				$ 0.00
SUBTOTAL =				$ 788.00
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. § 1.492(f)). +				$ 0.00
TOTAL NATIONAL FEE =				$ 788.00
Fee for recording the enclosed assignment (37 C.F.R. § 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. §§ 3.28, 3.31). **$40.00 per property** +				$ 0.00
TOTAL FEES ENCLOSED =				$ 788.00
				Amount to be refunded: $ 0.00
				charged: $ 1,758.00

a. ☒ A check in the amount of **$1,758.00** to cover the above fees is enclosed.

b. ☐ Please charge my **Deposit Account No. 03-1952** in the amount of $* to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Assistant Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment to **Deposit Account No. 03-1952**.

NOTE: Where an appropriate time limit under 37 C.F.R. § 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. § 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Thomas E. Ciotti
Morrison & Foerster LLP
755 Page Mill Road
Palo Alto, California 94304-1018

Thomas E. Ciotti
SIGNATURE

Thomas E. Ciotti
Registration No. 21,013

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420 Rec'd PCT/PTO 30 NOV 1999

19/PRTS

SPECIFICATION

SEMICONDUCTOR DEVICE AND DRIVING METHOD THEREOF

TECHNICAL FIELD

The present invention relates to a semiconductor device realized by a semiconductor element, such as a MOSFET, and a method of driving the same to operate in certain manners.

TECHNICAL BACKGROUND

A MOSFET controls electrical conduction between the source and drain by varying a voltage applied to the gate electrode. For example, in case of an N-type MOSFET, the conduction between the source and drain is allowed when a high level is inputted into the gate electrode, and stopped when a low level is inputted. Here, the

potential of the well is generally fixed. More specifically, the potential is fixed at the low level in the N-type MOSFET, and the high level in a P-type MOSFET. In this manner, the conventional MOSFET is used as a 3-terminal element which controls the switching between the source and drain by using the gate electrode as an input.

Figure 22 shows an example application of the above MOSFET by way of a circuit diagram of a logic circuit log1 as a typical conventional semiconductor device. The logic circuit log1 comprises (1) a pair of circuits of PMOSFETs (qp1 and qp2) in parallel, which are respectively provided with inputs in1 and in2 through input terminals p1 and p2, and connected to a high level V_{DD} power source line at one end and to an output terminal p3 at the other end, and (2) a pair of circuits of NMOSFETs (qn1 and qn2) in series, which are respectively provided with the inputs in1 and in2, and connected to the output terminal p3 at one end and to a low level GND power source line at the other end, thereby forming a NAND circuit which shifts its output OUT to the high level when at least one of the inputs in1 and in2 is in the low level.

Also, Figure 23 is a circuit diagram of a logic circuit log2 of another conventional semiconductor device. The logic circuit log2 comprises (1) a pair of

circuits of PMOSFETs (qp1 and qp2) in series, which are respectively provided with the inputs in1 and in2, and connected to the high level V_{DD} power source line at one end and to the output terminal p3 at the other end, and (2) a pair of circuits of NMOSFETs (qn1 and qn2) in parallel, which are respectively provided with the inputs in1 and in2, and connected to the output terminal p3 at one end and to the low level GND power source line at the other end, thereby forming a NOR circuit which shifts its output OUT to the low level when at least one of the inputs in1 and in2 is in the high level.

The logic circuits log1 and log2 representing the conventional semiconductor devices are arranged in such a manner that each MOSFET outputs one output in response to one input, and for this reason, the NAND circuit or NOR circuit demands four MOSFETs. Further, because an AND circuit is realized by connecting a NOT circuit (composed of two MOSFETs) to the NAND circuit in series, and an OR circuit is realized by connecting the NOT circuit to the NOR circuit in series, the AND circuit or OR circuit demands six MOSFETs. Accordingly, a large number of MOSFETs are necessary to run one operation, which makes it difficult to improve a packing density of the semiconductor device. Consequently, neither can the operating rate and yield be improved, nor the costs can

be reduced.

An object of the present invention is to provide a semiconductor device capable of improving a packing density by upgrading performance of each element, and increasing an operating rate and yield, while reducing the costs, and a driving method thereof.

DISCLOSURE OF THE INVENTION

A first semiconductor device of the present invention is furnished with:

a semiconductor substrate;

a background insulating film formed over the semiconductor substrate;

a P- or N-type semiconductor layer which is formed over the background insulating film and made into a first electrode, the semiconductor layer in each element being separated from the semiconductor layer in an adjacent element by means of an electrical insulating separation region encircling each element;

a source region and a drain region formed in the semiconductor layer and made into a second electrode and a third electrode, respectively, the source region and drain region having a conduction type opposite to a conduction type of the semiconductor layer;

a channel region formed between the source region

and drain region;

a gate insulating film formed over the channel region; and

a gate electrode formed as a fourth electrode on the gate insulating film,

wherein a contact hole is formed through the semiconductor layer for each element separated by means of the separation region, at a region other than the source region and drain region.

According to the above arrangement, by employing a substrate of an SOI (Silicon On Insulator) or SOS (Silicon On Sapphire) structure, in which elements are fabricated on the background insulating film formed over the semiconductor substrate, element forming regions for individual elements can be electrically separated from each other relatively easily by means of the separation region. Then, a MOSFET is formed in each separated element forming region under the conditions where each element is allowed to operate independently by preventing interference between the elements. Further, the semiconductor layer in each MOSFET is electrically connected to the outside through the contact hole, so that it can be used as an electrode, thereby realizing a 4-terminal element having two inputs: the input to the gate and the input to the semiconductor layer.

Consequently, a 2-input-1-output circuit can be realized by a single element, thereby upgrading the performance of the MOSFET itself. Accordingly, when a logic circuit is formed, not only can a packing density of an integrated circuit, an operating rate, and yield be improved, but also the costs can be reduced.

A second semiconductor device of the present invention is furnished with:

a semiconductor substrate;

a P- or N-type deep well region formed in the semiconductor substrate;

a shallow well region formed over the deep well region and made into a first electrode, a conduction type of the shallow well region being opposite to a conduction type of the deep well region;

a source region and a drain region formed in the shallow well region and made into a second electrode and a third electrode, respectively, the conduction type of the source region and drain region being opposite to a conduction type of the shallow well region;

a channel region formed between the source region and drain region;

a gate insulating film formed over the channel region; and

a gate electrode formed as a fourth electrode on the

gate insulating film, wherein:

at least the shallow well region in each element is electrically separated from the shallow well region in an adjacent element by means of a separation region; and

a contact hole is provided to the shallow well region in each element separated from the shallow well region in the adjacent element by means of the separation region, at a region other than the source region and drain region.

According to the above arrangement, by electrically isolating the shallow well region in each element forming region by means of the separation region, a MOSFET can be formed in each separated element forming region even when a bulk substrate is employed, so that each element can operate independently by preventing interference between the elements. Further, the shallow well region in each MOSFET is electrically connected to the outside through the contact hole, so that it can be used as an electrode, thereby realizing a 4-terminal element having two inputs: the input to the gate and the input to the shallow well region.

Consequently, a 2-input-1-output circuit can be realized by a single element, thereby upgrading the performance of the MOSFET itself. Accordingly, when a logic circuit is formed, not only can a packing density

of an integrated circuit, operating rate, and yield be improved, but also the costs can be saved. Moreover, the costs and resistance of the first electrode can be reduced further compared with a case where the SOI or SOS substrate is employed.

The first and second semiconductor devices are preferably arranged in such a manner that:

the elements having opposite conduction types are paired off;

a source of a P-type semiconductor element is fixed at a high potential, and a source of an N-type semiconductor element is fixed at a low potential;

gates of the P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

the contact holes in the P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drains of the P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

In this case, the CMOS inverter structure, in which, of the two MOSFETs of P- and N-types, the source of the PMOSFET is fixed at the high potential while the source of the NMOSFET is fixed at the low potential, and the

drains of the PMOSFET and NMOSFET are connected to each other, thereby to form an output, is further arranged such that the contact holes in the PMOSFET and NMOSFET are connected to each other, thereby to form the second input terminal, and the gates, namely the normal inputs, of the PMOSFET and NMOSFET are connected to each other, thereby to form the first input terminal.

Consequently, a NAND or NOR circuit can be realized by adequately adjusting potentials of the two inputs or impurity concentration in the channel region. Accordingly, the NAND or NOR circuit which conventionally demands four MOSFETs can be now realized by two MOSFETs.

Further, the first and second semiconductor devices are preferably arranged in such a manner that:

the elements having opposite conduction types are paired off;

a source of a P-type semiconductor element is fixed at a high potential, and a source of an N-type semiconductor element is fixed at a low potential;

both a gate of the P-type semiconductor element and the contact hole in the N-type semiconductor element form a first input terminal;

both a gate of the N-type semiconductor element and the contact hole in the P-type semiconductor element form a second input terminal; and

drains of both the N-type semiconductor element and P-type semiconductor element form an output terminal.

In this case, the CMOS inverter structure, in which, of a pair of a PMOSFET and an NMOSFET, the source of the PMOSFET is fixed at the high potential while the source of the NMOSFET is fixed at the low potential, and the drains of the PMOSFET and NMOSFET are connected to each other, thereby to form an output, is further arranged such that the gates of the PMOSFET and NMOSFET form the first and second input terminals, respectively, and the contact holes in the NMOSFET and PMOSFET also form the first and second input terminals, respectively.

Consequently, a NAND or NOR circuit can be realized by adequately adjusting potentials of the two inputs or impurity concentration in the channel region. Accordingly, the NAND or NOR circuit which conventionally demands four MOSFETs can be now realized by two MOSFETs.

Further, the first and second semiconductor devices are preferably arranged in such a manner that:

the elements having opposite conduction types are paired off;

a drain of an N-type semiconductor element is fixed at a high potential, and a drain of a P-type semiconductor element is fixed at a low potential;

gates of both the N-type semiconductor element and

P-type semiconductor element form a first input terminal;

the contact holes in both the N-type semiconductor element and P-type semiconductor element form a second input terminal; and

sources of both the N-type semiconductor element and P-type semiconductor element form an output terminal.

In this case, an AND or OR circuit can be realized by adequately adjusting potentials of the two inputs or impurity concentration in the channel region. Accordingly, the AND or OR circuit which conventionally demands six MOSFETs can be now realized by two MOSFETs.

Also, the first and second semiconductor devices are preferably arranged in such a manner that:

the elements having opposite conduction types are paired off;

a drain of an N-type semiconductor element is fixed at a high potential and a drain of a P-type semiconductor element is fixed at a low potential;

both a gate of the N-type semiconductor element and the contact hole in the P-type semiconductor element form a first input terminal;

both a gate of the P-type semiconductor element and the contact hole in the N-type semiconductor element form a second input terminal; and

drains of both the P-type semiconductor element and

N-type semiconductor element form an output terminal.

In this case, an AND or OR circuit can be realized by adequately adjusting potentials of the two inputs or impurity concentration in the channel region. Accordingly, the AND or OR circuit which conventionally demands six MOSFETs can be now realized by two MOSFETs.

The first and second semiconductor devices are preferably arranged further in such a manner that:

the gate and the contact hole are used as separate input terminals, into which different input signals synchronized to each other are inputted, respectively. In this case, each element outputs one output signal in response to two input signals synchronized to each other based on a clock or the like. Hence, not a simple ON/OFF operation of a 1-input-1-output circuit, but an operation of a 2-input-1-output logic circuit can be realized, and therefore, the logic circuit can be composed of a fewer elements.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross section of a semiconductor

element in accordance with a first embodiment of the present invention, showing a basic arrangement of the present invention;

Figure 2 is a graph showing an example of operating characteristics of the semiconductor element in Figure 1;

Figure 3 is a graph showing another example of the operating characteristics of the semiconductor element in Figure 1;

Figure 4 is a front view of a semiconductor element in accordance with a second embodiment of the present invention, showing a practical application of the arrangement in Figure 1;

Figure 5 is a perspective cross section taken on line V-V in Figure 4;

Figure 6 is a perspective cross section taken on line VI-VI in Figure 4;

Figure 7 is a front view of a semiconductor element in accordance with a third embodiment of the present invention, showing a practical application of the arrangement in Figure 1;

Figure 8 is a perspective cross section taken on line VIII-VIII in Figure 7;

Figure 9 is a perspective cross section taken on line IX-IX in Figure 7;

Figure 10 is a circuit diagram of a logic circuit in

accordance with a fourth embodiment of the present invention, in which the semiconductor element in any of Figures 1 through 9 is employed;

Figures 11(a) and 11(b) are graphs showing operating characteristics of the logic circuit in Figure 10;

Figure 12 is a circuit diagram of a logic circuit in accordance with a fifth embodiment of the present invention, in which the semiconductor element in any of Figures 1 through 9 is employed;

Figures 13(a) and 13(b) are graphs showing operating characteristics of the logic circuit in Figure 12;

Figures 14(a) and 14(b) are graphs showing operating characteristics of a logic circuit in accordance with a sixth embodiment of the present invention;

Figures 15(a) and 15(b) are graphs showing operating characteristics of a logic circuit in accordance with a seventh embodiment of the present invention;

Figure 16 is a circuit diagram of a logic circuit in accordance with an eighth embodiment of the present invention, in which the semiconductor element in any of Figures 1 through 9 is employed;

Figures 17(a) and 17(b) are graphs showing operating characteristics of the logic circuit in Figure 16;

Figure 18 is a circuit diagram of a logic circuit in accordance with a ninth embodiment of the present

invention, in which the semiconductor element in any of Figures 1 through 9 is employed;

Figures 19(a) and 19(b) are graphs showing operating characteristics of the logic circuit in Figure 18;

Figures 20(a) and 20(b) are graphs showing operating characteristics of a logic circuit in accordance with a tenth embodiment of the present invention;

Figures 21(a) and 21(b) are graphs showing operating characteristics of a logic circuit in accordance with an eleventh embodiment of the present invention;

Figure 22 is a circuit diagram showing an example of a logic circuit composed of typical conventional MOSFET elements; and

Figure 23 is a circuit diagram showing another example of the logic circuit composed of typical conventional MOSFET elements.

THE MOST PREFERRED EMBODIMENT OF THE INVENTION

The following will describe in detail the present invention with reference to accompanying drawings. Initially, referring to Figures 1 through 3, the following description will describe a first embodiment of the present invention.

Figure 1 is a cross section schematically showing a semiconductor element 1 in accordance with the first

embodiment of the present invention to explain a basic arrangement of the present invention. As shown in the drawing, in addition to a typical MOSFET structure, in which a source region 3 and a drain region 4 are formed in a well 2, and a gate electrode 7 is fabricated on a channel region 5 formed between the source region 3 and drain region 4 through a gate insulating film 6, the semiconductor element 1 has a 4-terminal structure, in which: a substrate terminal TW is pulled out from the well 2 through a contact hole (not shown) and made into a first electrode; a source terminal TS is pulled out from the source region 3 and made into a second electrode; a drain terminal TD is pulled out from the drain region 4 and made into a third electrode; and a gate terminal TG is pulled out from the gate electrode 7 and made into a fourth electrode. The gate terminal TG as the first input terminal and the substrate terminal TW as the second input terminal respectively receive inputs IN1 and IN2, which are different signals synchronized to each other based on a clock signal or the like. Here, an appropriate drain voltage is applied across the drain and source.

In case that the semiconductor element 1 is an NMOSFET (having the well 2 of P-type), the relation of a drain current with respect to the potentials of the

inputs IN1 and IN2 is as the one shown in Figure 2. When the input IN2 (well potential) has a low potential (L), and the input IN1 (gate potential) has the low potential (L), I_{LL} is yielded as the drain current. When the input IN2 has the low potential (L), and the input IN1 has a high potential (H), I_{HL} is yielded as the drain current.

In contrast, when the input IN2 has the high potential (H) and the input IN1 has the low potential (L), I_{LH} is yielded as the drain current. When the input IN2 has the high potential (H), and the input IN1 also has the high potential (H), I_{HH} is yielded as the drain current.

As has been discussed above, with respect to the same input IN1, the drain current becomes larger with the input IN2 having a higher potential. This is because, in the MOSFET, when a positive voltage is applied to the well 2, a potential barrier in the channel region is reduced, and so is a threshold voltage.

Figure 2 reveals that when the input IN2 has the low potential (L), more or less the same drain current is yielded whether the input IN1 has the high potential (H) or low potential (L), but when the input IN2 has the high potential (H), the drain current varies considerably depending on whether the input IN1 has the high potential (H) or low potential (L). Hence, the example case shown

in Figure 2 realizes an operation such that the conduction between the drain and source is allowed only when both of the inputs IN1 and IN2 have the high potential (H), and stopped otherwise.

On the other hand, by setting the operating characteristics as shown in Figure 3, an operation can be realized such that the conduction between the source and drain is allowed when at least one of the inputs IN1 and IN2 has the high potential (H), and stopped only when both of the inputs IN1 and IN2 have the low potential (L).

The characteristics shown in Figures 2 and 3 can be selected with the semiconductor element 1 arranged in the manner as shown in Figure 1 by, for example, adequately adjusting impurity concentration in the channel region 5, or the levels of the high potential (H) and low potential (L) of the inputs IN1 and IN2. It should be appreciated that in case that the semiconductor element 1 is a PMOSFET (having the well 2 of N-type), the operating characteristics are opposite to those shown in Figures 2 and 3.

Consequently, a packing density of an integrated circuit can be improved by upgrading the performance of a single element capable of outputting one output in response to two different inputs IN1 and IN2 synchronized

to each other.

Referring to Figures 4 through 6, the following description will describe a second embodiment of the present invention.

Figures 4 through 6 are views showing an arrangement of a semiconductor element 11, which is a practical application of the semiconductor element 1. Figure 4 is a front view. Figure 5 is a perspective cross section taken on line V-V in Figure 4, and Figure 6 is a perspective cross section taken on line VI-VI in Figure 4. Figure 4 omits top metal wires and an inter-layer insulating film hereinafter referred to and shows only a substantial part of the element for ease of explanation.

The semiconductor element 11 employs an SOI substrate composed of a semiconductor substrate 12, on which a background insulating layer 13 and a semiconductor layer 14 are formed sequentially in a vertical direction. The semiconductor layer 14 (well 2) in each element is electrically separated from the one in the adjacent element by means of a field oxide film 15, so that a change in well potential between the adjacent elements will not give any adverse effect. The source region 3 and drain region 4 are formed in the semiconductor layer 14. The conduction type of the source region 3 and drain region 4 is opposite to that of

the semiconductor layer 14. For example, when the semiconductor element 11 is an NMOSFET, the semiconductor layer 14 is of the P-type, and the source region 3 and drain region 4 are of the N-type. The gate electrode 7 is fabricated on the channel region formed between the source region 3 and drain region 4 through the gate insulating film 6.

The element thus formed is covered with an inter-layer insulating film 16. Contact holes 17, 18, and 19 are formed through the inter-layer insulating film 16, so that top metal wires 21, 22, and 23 are electrically connected to the source region 3, drain region 4, and gate electrode 7, respectively (see Figures 5 and 6), whereby the top metal wires 21, 22, and 23 form the source terminal TS, drain terminal TD, and the gate terminal TG as the first input terminal, respectively. Another contact hole 20 is formed through the inter-layer insulating film 16 at a region other than the source region 3 and drain region 4 (see Figure 6). A region 14a in the semiconductor layer 14 corresponds to the contact hole 20, and has the same conduction type as that of the semiconductor layer 14 and high impurity concentration. The region 14a establishes an ohmic contact between the top metal wire 24 formed inside the contact hole 20 and the semiconductor layer 14, so that the top metal wire 24

forms the substrate terminal TW as the second input terminal.

According to the above arrangement, a 4-terminal element, such as the one shown in Figure 1, can be realized by electrically separating the adjacent elements relatively easily by merely employing an SOI substrate and forming the field oxide film 15 in the semiconductor layer 14.

As has been discussed, the present embodiment is arranged in such a manner that: element forming regions are electrically separated by means of a separation region (field oxide film 15) on the SOI or SOS structure substrate, and a MOSFET is formed in each separated element forming region; and then, the semiconductor layer in each MOSFET is connected to the outside through the contact hole, so that it can be used as an electrode.

The above arrangement realizes a 2-input-1-output circuit by a single element, thereby upgrading the performance of the MOSFET itself. Consequently, when a logic circuit is assembled, not only can a packing density of an integrated circuit be improved, but also the operating rate and yield can be increased while the costs can be reduced.

Referring to Figures 7 through 9, the following description will describe a third embodiment of the

present invention.

Figures 7 through 9 are views showing an arrangement of a semiconductor element 31, which is another practical application of the semiconductor element 1 in Figure 1 in a different structure (bulk type structure) from the semiconductor element 11 in Figures 4 through 6. Figure 7 is a front view. Figure 8 is a perspective cross section taken on line VIII-VIII in Figure 7, and Figure 9 is a perspective cross section taken on line IX-IX in Figure 7. Figure 7 omits an inter-layer insulating film and top metal wires for ease of explanation.

The semiconductor element 31 uses a substrate composed of a semiconductor substrate 32, on which a deep well region 33 and a shallow well region 34 having a conduction type opposite to that of the deep well region 33 are layered sequentially in a vertical direction. A heavily doped region 35 is formed in the shallow well region 34 so as to reduce resistance of the same. Each element is electrically separated from the adjacent element by means of an electrical insulating separation region 36. The shallow well region 34 is provided with the source region 3 and drain region 4 of the conduction type opposite to that of the shallow well region 34. Also, the gate electrode 7 is fabricated on the channel region, formed between the source region 3 and drain

region 4, through the gate insulating film 6. It should be appreciated that the layer formed between the heavily doped region 35 and deep well region 33 is the shallow well region.

The source region 3, drain region 4, and gate electrode 7 are electrically connected to top metal wires 45, 46, and 47 respectively via contact holes 41, 42, and 43 formed through an inter-layer insulating film 37. The shallow well region 34 is provided with a region 34a which is heavily doped with impurities, at a region other than the source region 3 and drain region 4. The region 34a is electrically connected to a top metal wire 48 via a contact hole 44 formed through the inter-layer insulating film 37 (see Figure 9), whereby an ohmic contact is established between the shallow well region 34 and top metal wire 48. Also, a field oxide film 38 is formed between the region 34a and gate electrode 7. (see Figure 9).

The depth and impurity concentration of the source region 3 and drain region 4 in the semiconductor element 31 are approximately 100nm and $1 \times 10^{20}/cm^3$ or greater, and those of the shallow well region 34 are approximately 1,000nm and $5 \times 10^{16}/cm^3$ to $1 \times 10^{17}/cm^3$. The depth of the heavily doped region 35 at which the distribution of the impurity concentration reaches its peak is 500nm to

700nm, and the peak concentration is approximately $1 \times 10^{18}/cm^3$ to $1 \times 10^{19}/cm^3$. Also, the depth and the impurity concentration of the deep well region 33 are approximately 3 μm and $5 \times 10^{16}/cm^3$. It should be appreciated, however, that the depth and concentration of impurity of each region are not limited to the foregoing.

Here, the shallow well region 34 can be electrically isolated from the one in the adjacent element by setting the depth of the separation region 36 to at least a sum of the depth of the shallow well region 34 and the width of a depletion layer formed at the junction between the shallow well region 34 and deep well region 33 (to be more accurate, the width of the depletion layer on a portion extending toward the deep well region 33). In contrast, if the depth of the separation region 36 is shorter than the sum of the depth of the shallow well region 34 and the width of the depletion layer formed at the junction between the shallow well region 34 and deep well region 33, conduction between the shallow well regions 33 in the adjacent elements is allowed by means of the depletion layer at the deep well region 33 side, thereby causing unwanted punch-through.

Thus, according to the above arrangement, the adjacent elements can be electrically isolated from each other by providing the separation region 36 that causes

a slight increasing of the space which is almost as small as the smallest processable dimensions. Consequently, a bulk type of the 4-terminal semiconductor element 1 as shown in Figure 1 can be realized by omitting an expensive SOI substrate having high body resistance.

As has been discussed, the present embodiment is arranged in such a manner that: a bulk substrate, in which the deep well region of either P- or N-type and the shallow well region of the other conduction type are formed in the semiconductor substrate, and at least the shallow well region in each element is electrically separated from the one in the adjacent element by means of the separation region, is used; and a MOSFET is formed in each separated element forming region while the shallow well region is electrically connected to the outside through the contact hole provided at a region other than the source region and drain region of the MOSFET, so that the shallow well region can be used as an electrode.

Consequently, even when a bulk substrate is employed, each element can operate independently by preventing unwanted interference between the elements by electrically isolating the shallow well region in each element forming region by means of the separation region. In addition, the shallow well region in the MOSFET is

electrically connected to the outside through the contact hole so as to be used as an electrode. Consequently, the above arrangement realizes two inputs: one into the gate and the other into the semiconductor layer.

Moreover, because a 2-input-1-output circuit can be realized by a single element, the performance of the MOSFET itself can be upgraded. Thus, when a logic circuit is assembled, for example, not only the packing density of an integrated circuit can be improved, but also the operating rate and yield can be increased while the costs can be saved. In addition, compared with a case employing an SOI or SOS substrate, the costs and the resistance of the first electrode can be reduced further.

Referring to Figures 10 and 11, the following description will describe a fourth embodiment of the present invention.

Figure 10 shows a practical application of a unit element, namely, the semiconductor element 1, 11, or 31 by way of a circuit diagram of a logic circuit LOG1 of the CMOS structure. In addition to a typical CMOS inverter structure comprising a pair of a PMOSFET (QP) and a NMOSFET (QN), in which the source TSP of the PMOSFET (QP) is connected to a high level (V_{DD}) power source line and the source TSN of the NMOSFET (QN) is connected to a low level (GND) power source line, and the

drains TDP and TDN of these MOSFETs (QP and QN) are both connected to the output terminal P3, while the gates TGP and TGN thereof are both connected to the first input terminal P1, the logic circuit LOG1 has an arrangement such that the substrate terminals TWP and TWN of these MOSFETs (QP and QN) are both connected to the second input terminal P2.

In addition, by adequately selecting the power source voltage V_{DD} and impurity concentration in the channel region, the operating characteristics of the drain current with respect to the inputs IN1 and IN2 of the PMOSFET (QP) are set as shown in Figure 11(a) and those of the NMOSFET (QN) in Figure 11(b). In other words, each MOSFET (QP and QN) is arranged in such a manner that, when the input IN2 has the low potential (L), a threshold voltage (at the break point in the graph) becomes higher than the high potential (H), and when the input IN2 has the high potential (H), the threshold voltage becomes lower than the high potential (H) and higher than the low potential (L).

In the above-arranged logic circuit LOG1, when the input IN1 has the low potential (L), the PMOSFET (QP) conducts and NMOSFET (QN) stops conducting regardless of the potential of the input IN2, whereby the output OUT has the high potential (H). In contrast, when the input

IN1 has the high potential (H), the PMOSFET (QP) conducts and the NMOSFET (QN) stops conducting if the input IN2 has the low potential (L), whereby the output OUT has the high potential (H). On the other hand, if the input IN2 has the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts, whereby the output OUT has the low potential (L). The foregoing operations are set forth in Table 1 below. It is understood from Table 1 below that the logic circuit LOG1 realizes a NAND operation, in which the output OUT has the low potential (L) only when both of the inputs IN1 and IN2 have the high potential (H), and the high potential (H) when at least one of the inputs IN1 and IN2 has the low potential (L).

Table 1

IN1	IN2	QP	QN	OUT
L	L	ON	OFF	H
L	H	ON	OFF	H
H	L	ON	OFF	H
H	H	OFF	ON	L

Consequently, a NAND circuit which typically demands four MOSFETs can be now realized by two MOSFETs, thereby improving a packing density of the integral circuit in a reliable manner by upgrading the performance of each

element.

As has been discussed, the present embodiment is arranged in such a manner that, in the CMOS inverter structure having a pair of elements of opposite conduction types, the contact holes in these elements form the second input terminal, and the gates, namely the normal inputs, of these elements form the first input terminal.

Consequently, the NAND circuit can be realized by adequately adjusting the potentials of the two inputs or the impurity concentration in the channel region, and the NAND or NOR circuit which conventionally demands four MOSFETs can be now realized by two MOSFETs.

Referring to Figures 12 and 13, the following description will describe a fifth embodiment of the present invention.

Figure 12 is a circuit diagram of a logic circuit LOG2 in accordance with the fifth embodiment of the present invention. The logic circuit LOG2 is similar to the logic circuit LOG1 in that it includes a pair of MOSFETs of P-type (QP) and N-type (QN), and the source TSP of the PMOSFET (QP) is connected to the high level (V_{DD}) power source line, while the source TSN of the NMOSFET (QN) is connected to the low level (GND) power source line, and the drains TDP and TDN of these MOSFETs

are both connected to the output terminal P3. However, the logic circuit LOG2 is different from the logic circuit LOG1 in the followings. That is, the gate TGP of the PMOSFET (QP) and the substrate terminal TWN of the NMOSFET (QN) are both connected to the input terminal P1, and the gate TGN of the NMOSFET (QN) and the substrate terminal TWP of the PMOSFET (QP) are both connected to the input terminal P2.

The operating characteristics of the logic circuit LOG2 are set as shown in Figure 13. In other words, as shown in Figure 13(a), the PMOSFET (QP) is arranged in such a manner that, when the input IN2 (well potential) has the low potential (L), the threshold voltage becomes higher than the high potential (H), and when the input IN2 has the high potential (H), the threshold voltage becomes lower than the high potential (H) and higher than the low potential (L). In contrast, as shown in Figure 13(b), the NMOSFET (QN) is arranged in such a manner that, when the input IN1 has the low potential (L), the threshold voltage becomes higher than the high potential (H), and when the input IN1 has the high potential (H), the threshold voltage becomes lower than the high potential (H) and higher than the low potential (L).

Thus, when the input IN1 has the low potential (L), the PMOSFET (QP) conducts and the NMOSFET stops

conducting regardless of the level of the input IN2, whereby the output OUT has the high potential (H). Also, when the input IN1 has the high potential (H), if the input IN2 has the low potential (L), the PMOSFET (QP) conducts and the NMOSFET (QN) stops conducting, whereby the output OUT has the high potential (H). Further, when both of the inputs IN1 and IN2 have the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts, whereby the output OUT has the low potential (L).

In other words, as set forth in Table 1 above, the output OUT has the low potential (L) only when both of the inputs IN1 and IN2 have the high potential (H), and the high potential (H) otherwise. The aforementioned NAND operation can be also realized by the above arrangement.

As has been described, the present embodiment is arranged in such a manner that, in the CMOS inverter structure having a pair of elements of opposite conduction types, the gates of the PMOSFET and NMOSFET form the first and second input terminals, respectively, and the contact holes in the NMOSFET and PMOSFET also form the first and second input terminals, respectively.

Thus, by adequately adjusting the potentials of the two inputs or impurity concentration in the channel

region, the NAND circuit can be realized. Consequently, the NAND circuit which conventionally demands four MOSFETs can be now realized by two MOSFETs.

Referring to Figure 14, the following description will describe a sixth embodiment of the present invention.

In the present embodiment, the operating characteristics of the MOSFETs (QP and QN) in the logic circuit LOG1 shown in Figure 10 are not set as shown in Figures 11(a) and 11(b), but as shown in Figures 14(a) and 14(b). In other words, each MOSFET (QP and QN) is arranged in such a manner that the threshold voltage becomes higher than the lower potential (L) and lower than the high potential (H) when the input IN2 has the low potential (L), and lower than the low potential (L) when the input IN2 has the high potential (H).

Accordingly, when the input IN1 has the high potential (H), the PMOSFET (QP) stops conducting and NMOSFET (QN) conducts regardless of the potential of the input IN2, whereby the output OUT has the low potential (L). When the input IN1 has the low potential (L) and the input IN2 has the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts, whereby the output OUT also has the low potential (L). Further, when both of the inputs IN1 and IN2 have the low

potential (L), the PMOSFET (QP) conducts and the NMOSFET (QN) stops conducting, whereby the output OUT has the high potential (H). The foregoing operations are set forth in Table 2 below, and the logic circuit LOG1 can realize a NOR operation, in which the output OUT has the high potential (H) only when both of the inputs IN1 and IN2 have the low potential (L), and the low potential (L) otherwise.

Table 2

IN1	IN2	QP	QN	OUT
L	L	ON	OFF	H
L	H	OFF	ON	L
H	L	OFF	ON	L
H	H	OFF	ON	L

As has been discussed, the NOR circuit which generally demands four MOSFETs can be now realized by two MOSFETs.

Referring to Figure 15, the following description will describe a seventh embodiment of the present invention.

Figure 15 is a graph showing the operating characteristics in accordance with the seventh embodiment of the present invention, which are adapted to the logic circuit LOG2 shown in Figure 12. Figure 15(a) shows the

operating characteristics of the PMOSFET (QP) and Figure 15(b) shows those of the NMOSFET (QN). In other words, each MOSFET is arranged in such a manner that, when both of the well potential (input IN2) of the PMOSFET (QP) and the well potential (input IN1) of the NMOSFET have the low potential (L), the threshold voltage becomes higher than the low potential (L) and lower than the high potential (H), and when the well potential in each MOSFET has the high potential (H), the threshold voltage becomes lower than the low potential (L).

Thus, when the input IN1 has the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts regardless of the potential of the input IN2, whereby the output OUT has the low potential (L). Also, when the input IN1 has the low potential (L) and the input IN2 has the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts, whereby the output OUT also has the low potential (L). Further, when both of the inputs IN1 and IN2 have the low potential (L), the PMOSFET (QP) conducts and the NMOSFET (QN) stops conducting, whereby the output OUT has the high potential (H).

Thus, the above arrangement can also realize the NOR operation set forth in Table 2 above, in which the output OUT has the high potential (H) only when both of the

inputs IN1 and IN2 have the low potential (L), and the low potential (L) otherwise.

Referring to Figures 16 and 17, the following description will describe an eighth embodiment of the present invention.

Figure 16 is a circuit diagram of a logic circuit LOG3 in accordance with the eighth embodiment of the present invention. In the logic circuit LOG3, the drain TDN of the NMOSFET (QN) is connected to the high level (V_{DD}) power source line, and the drain TDP of the PMOSFET (QP) is connected to the low level (GND) power source line. Also, the sources TSP and TSN of theses MOSFETs (QP and QN) are both connected to the output terminal P3, and the gates TGP and TGN of the same are both connected to the first input terminal P1, while the substrate terminals TWP and TWN of the same are both connected to the second input terminal P2.

By adequately selecting the power source voltage V_{DD} or impurity concentration in the channel region, the operating characteristics of the drain current with respect to the inputs IN1 and IN2 of the PMOSFET (QP) are set forth in Figure 17(a) and those of the NMOSFET (QN) in Figure 17(b).

In other words, each MOSFET (QP and QN) is arranged in such a manner that, when the input IN2 (well

potential) has the low potential (L), the threshold voltage becomes higher than the high potential (H), and when the input IN2 has the high potential (H), the threshold voltage becomes lower than the high potential (H) and higher than the low potential (L).

Thus, when the input IN1 has the low potential (L), the PMOSFET (QP) conducts and the NMOSFET stops conducting regardless of the potential of the input IN2, whereby the output OUT has the low potential (L). Also, when the input IN1 has the high potential (H), even if the input IN2 has the low potential (L), the PMOSFET (QP) conducts and the NMOSFET (QN) stops conducting, whereby the output OUT has the low potential (L). Further, when both of the inputs IN1 and IN2 have the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts, whereby the output OUT has the high potential (H).

Thus, the logical circuit LOG3 can realize an AND operation as set forth in Table 3 below, in which the output OUT has the high potential (H) only when both of the inputs IN1 and IN2 have the high potential (H), and low potential (L) otherwise.

Table 3

IN1	IN2	QP	QN	OUT
L	L	ON	OFF	L
L	H	ON	OFF	L
H	L	ON	OFF	L
H	H	OFF	ON	H

Consequently, an AND circuit which generally demands six MOSFETs as described in the "Technical Background" column can be now realized by two MOSFETs.

As has been discussed, the present embodiment is arranged in such a manner that: the elements of opposite conduction types are paired off; the drain of the N-type semiconductor element is fixed at the high potential, and the drain of the P-type semiconductor element is fixed at the low potential; the gates of both the elements form the first input terminal; and the contact holes in the same form the second input terminal.

Thus, by adequately adjusting the potentials of the two inputs or impurity concentration in the channel region, the AND circuit can be realized. Consequently, the AND circuit which conventionally demands six MOSFETs can be now realized by two MOSFETs.

Referring to Figures 18 and 19, the following description will describe a ninth embodiment of the present invention.

Figure 18 is a circuit diagram of a logic circuit LOG4 in accordance with the ninth embodiment of the present invention. The logic circuit LOG4 is similar to the logic circuit LOG3 described above in that: the drain TDN of the NMOSFET (QN) is connected to the high level (V_{DD}) power source line, and the drain TDP of the PMOSFET (QP) is connected to the low level (GND) power source line; and the sources TSP and TSN of these MOSFETs are both connected to the output terminal P3. However, the logic circuit LOG4 is different from the logic circuit LOG3 in the following. That is, the gate TGN of the NMOSFET (QN) and the substrate terminal TWP of the PMOSFET (QP) are both connected to the input terminal P1, and the gate TGP of the PMOSFET (QP) and the substrate terminal TWN of the NMOSFET (QN) are both connected to the input terminal P2.

Also, the operating characteristics of the logic circuit LOG4 are set as shown in Figure 19. To be more specific, as shown in Figure 19(a), the PMOSFET (QP) is arranged in such a manner that the threshold voltage becomes higher than the high potential (H) when the input IN1 (well potential) has the low potential (L), and lower than the high potential (H) and higher than the low potential (L) when the input IN1 has the high potential (H). In contrast, as shown in Figure 19(b), the NMOSFET

(QN) is arranged in such a manner that the threshold voltage becomes higher than the high potential (H) when the input IN2 has the low potential (L), and lower than the high potential (H) and higher than the low potential (L) when the input IN2 has the high potential (H).

Thus, when the input IN1 has the low potential (L), the PMOSFET (QP) conducts and the NMOSFET (QN) stops conducting regardless of the level of the input IN2, whereby the output OUT has the low potential (L). When the input IN1 has the high potential (H), the PMOSFET (QP) conducts and the NMOSFET stops conducting if the input IN2 has the low potential (L), whereby the output OUT has the low potential (L). Further, when both of the inputs IN1 and IN2 have the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts, whereby the output OUT has the high potential (H).

In other words, the above arrangement can also realize the AND operation as set forth in Table 3 above, in which the output OUT has the high potential (H) only when both of the inputs IN1 and IN2 have the high potential (H), and the low potential (L) otherwise.

As has been discussed, the present embodiment is arranged in such a manner that: the elements of opposite conduction types are paired off; the drain of the N-type

semiconductor element is fixed at the high potential, and the drain of the P-type semiconductor is fixed at the low potential; both the gate of the N-type semiconductor element and the contact hole in the P-type semiconductor element form the first input terminal; both the gate of the P-type semiconductor element and the contact hole in the N-type semiconductor element form the second input terminal; and the drains of both the MOSFETs form the output terminal.

Thus, by adequately adjusting the potentials of the two inputs or impurity concentration in the channel region, the AND circuit can be realized. Consequently, the AND circuit which conventionally demands six MOSFETs can be now realized by two MOSFETs.

Referring to Figure 20, the following description will describe a tenth embodiment of the present invention.

Figure 20 is a graph showing the operating characteristics of the tenth embodiment of the present invention, which are adapted to the logic circuit LOG3 of Figure 16. Figure 20(a) shows the operating characteristics of the PMOSFET (QP) and Figure 20(b) shows those of the NMOSFET (QN). Each MOSFET (QP and QN) is arranged in such a manner that, when the well potential (input IN2) has the low potential (L), the

threshold voltage becomes higher than the low potential (L) and lower than the high potential (H), and lower than the low potential (L) when the input IN2 has the high potential (H).

Thus, when the input IN1 has the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts regardless of the potential of the input IN2, whereby the output OUT has the high potential (H). Also, when the input IN1 has the low potential (L) and the input IN2 has the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts, whereby the output OUT also has the high potential (H). Further, when both of the inputs IN1 and IN2 have the low potential (L), the PMOSFET (QP) conducts and the NMOSFET (QN) stops conducting, whereby the output OUT has the low potential (L).

In other words, it is understood that the above arrangement can realize an OR operation as set forth in Table 4 below, in which the output OUT has the low potential (L) only when both of the inputs IN1 and IN2 have the low potential (L), and the high potential (H) otherwise.

Table 4

IN1	IN2	QP	QN	OUT
L	L	ON	OFF	L
L	H	OFF	ON	H
H	L	OFF	ON	H
H	H	OFF	ON	H

Consequently, an OR circuit which generally demands six MOSFETs as previously described can be now realized by two MOSFETs.

Referring to Figure 21, the following description will describe an eleventh embodiment of the present invention.

Figure 21 is a graph showing the operating characteristics of the eleventh embodiment of the present invention, which are adapted to the logic circuit LOG4 of Figure 18. Figure 21(a) shows the operating characteristics of the PMOSFET (QP) and Figure 21(b) shows those of the NMOSFET (QN). In other words, each MOSFET is arranged in such a manner that, when the well potential (input IN1) of the PMOSFET (QP) and the well potential (input IN2) of the NMOSFET (QN) have the low potential (L), the threshold voltage becomes higher than the low potential (L) and lower than the high potential (H), and when the well potential in each MOSFET has the high potential (H), the threshold voltage becomes lower

than the low potential (L).

Thus, when the input IN1 has the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET conducts regardless of the potential of the input IN2. Also, when the input IN1 has the low potential (L) and the input IN2 has the high potential (H), the PMOSFET (QP) stops conducting and the NMOSFET (QN) conducts, whereby the output OUT also has the high potential (H). Further, when both of the inputs IN1 and IN2 have the low potential (L), the PMOSFET (QP) conducts and the NMOSFET (QN) stops conducting, whereby the output OUT has the low potential (L).

In other words, the above arrangement can also realize the OR operation as set forth in Table 4 above, in which the output OUT has the low potential (L) only when the inputs IN1 and IN2 have the low potential (L), and the high potential (H) otherwise.

As has been discussed, the present embodiment is arranged in such a manner that the gate and contact hole form the separate input terminals, into which input signals synchronized to each other based on a clock or the like are inputted, respectively.

Consequently, the above arrangement does not realize a simple ON/OFF operation of the 1-input-1-output circuit, but an operation of the 2-input-1-output logic

circuit, thereby making it possible to assemble the logic circuit with a fewer elements.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

INDUSTRIAL APPLICABILITY

As has been discussed, the semiconductor device of the present invention is useful as logical operation circuits of various kinds, and particularly suitable to logical operation circuits for which a packing density should be improved by upgrading the performance of each element, and the operating rate and yield should be increased while reducing the costs.

SCOPE OF CLAIMS

1. A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others; and

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region.

2. The semiconductor device of Claim 1, wherein operating characteristics are changed by adjusting impurity concentration in said channel region and levels of a high voltage and a low voltage applied to said gate terminal and substrate terminal.

3. The semiconductor device of Claim 1, wherein said semiconductor layer in each of said semiconductor elements is electrically separated from each other by

means of an oxide film.

4. A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said semiconductor layer is composed of a shallow well region, a heavily doped region for reducing resistance of said shallow well region, and a deep well region, which are sequentially layered in a vertical direction; and

said semiconductor layer is provided with a substrate terminal through a contact hole at a region other than said source region and drain region.

5. The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is electrically separated from the others by means of a separation region; and

a depth of said separation region is set at least as

large as a sum of a depth of said shallow well region and a width of a depletion layer formed at a junction of said shallow well region and deep well region.

6. The semiconductor device of Claim 1, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

7. The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type

semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

8. The semiconductor device of Claim 6, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

9. The semiconductor device of Claim 7, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

10. The semiconductor device of Claim 1, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a

second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

11. The semiconductor device of Clam 4, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

12. The semiconductor device of Claim 10, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential.

13. The semiconductor device of Claim 11, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in

such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential.

14. The semiconductor device of Claim 6, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

15. The semiconductor device of Claim 7, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high

potential.

16. The semiconductor device of Claim 10, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential.

17. The semiconductor device of Claim 11, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low

potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential.

18. The semiconductor device of Claim 1, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a drain terminal of said N-type semiconductor element is supplied with a high potential and a drain terminal of said P-type semiconductor element is supplied with a low potential;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

source terminals of said P-type semiconductor element and N-type semiconductor element are connected to

each other, thereby to form an output terminal.

19. The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a drain terminal of said N-type semiconductor element is supplied with a high potential and a drain terminal of said P-type semiconductor element is supplied with a low potential;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

source terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

20. The semiconductor device of Claim 18, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied

with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

21. The semiconductor device of Claim 19, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

22. The semiconductor device of Claim 1, wherein:

each of said semiconductor elements is composed of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a drain terminal of said N-type semiconductor element and a low potential is supplied to a drain terminal of said P-type semiconductor element;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor

element are connected to each other, thereby to form a first input terminal;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

23. The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a drain terminal of said N-type semiconductor element and a low potential is supplied to a drain terminal of said P-type semiconductor element;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a

second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

24. The semiconductor device of Claim 22, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

25. The semiconductor device of Claim 23, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal

is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

26. The semiconductor device of Claim 18, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

27. The semiconductor device of Claim 19, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that

a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

28. The semiconductor device of Claim 22, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential.

29. The semiconductor device of Claim 23, wherein:

said P-type semiconductor element is arranged in

such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential.

30. A semiconductor device comprising:

a semiconductor substrate;

a background insulating film formed over said semiconductor substrate;

a semiconductor layer of P- or N-type which is formed over said background insulating film and made into a first electrode, each element in said semiconductor layer being separated from an adjacent element by means of an insulating separation region which encircles each element;

a source region and a drain region which are formed

in said semiconductor layer and made into a second electrode and a third electrode, respectively, a conduction type of each being opposite to a conduction type of said semiconductor layer;

a channel region formed between said source region and drain region;

a gate insulating film formed over said channel region; and

a gate electrode formed as a fourth electrode on said gate insulating film,

said semiconductor device being characterized in that said semiconductor layer is separated by means of said separation region, and a contact hole is formed through said each semiconductor layer separated by means of said separation region, at a region other than said source region and drain region.

31. A semiconductor device comprising:

a semiconductor substrate;

a deep well region of P- or N-type formed in said semiconductor substrate;

a shallow well region which is formed over said deep well region and made into a first electrode, a conduction type of said shallow well region being opposite to a conduction type of said deep well region;

a source region and a drain region of P- or N-type which are formed in said shallow well region and made into a second electrode and a third electrode, respectively;

a channel region formed between said source region and drain region;

a gate insulating film formed over said channel region; and

a gate electrode formed as a fourth electrode on said gate insulating film,

said semiconductor device being characterized in that:

at least said shallow well region in each element is electrically separated from the shallow well region in an adjacent element by means of a separation region; and

a contact hole is provided to said shallow well region in each element separated from the shallow well region in the adjacent element by means of said separation region, at a region other than said source region and drain region.

32. The semiconductor device of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a source of a P-type semiconductor element is fixed at a high potential and a source of an N-type semiconductor element is fixed at a low potential;

gates of both said P-type semiconductor element and N-type semiconductor element form a first input terminal;

said contact holes in both said P-type semiconductor element and N-type semiconductor element form a second input terminal; and

drains of both said P-type semiconductor element and N-type semiconductor element form an output terminal.

33. The semiconductor device of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a source of a P-type semiconductor element is fixed at a high potential and a source of an N-type semiconductor element is fixed at a low potential;

a gate of said P-type semiconductor element and said contact hole in said N-type semiconductor element form a first input terminal;

both a gate of said N-type semiconductor element and said contact hole in said P-type semiconductor element form a second input terminal;

drains of both said P-type semiconductor element and

N-type semiconductor element form an output terminal.

34. The semiconductor element of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a drain of an N-type semiconductor element is fixed at a high potential and a drain of a P-type semiconductor element is fixed at a low potential;

gates of both said N-type semiconductor element and P-type semiconductor element form a first input terminal;

said contact holes in both said N-type semiconductor element and P-type semiconductor element form a second input terminal; and

sources of both said N-type semiconductor element and P-type semiconductor element form an output terminal.

35. The semiconductor element of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a drain of an N-type semiconductor element is fixed at a high potential and a drain of a P-type semiconductor element is fixed at a low potential;

both a gate of said N-type semiconductor element

and said contact hole in said P-type semiconductor element form a first input terminal;

both a gate of said P-type semiconductor element and said contact hole in said N-type semiconductor element form a second input terminal; and

drains of both said P-type semiconductor element and N-type semiconductor element form an output terminal.

36. A method of driving the semiconductor device in any of Claims 30 through 35 characterized in that said gate and said contact hole form separate input terminals, into which different input signals synchronized to each other are inputted respectively.

ABSTRACT OF THE DISCLOSURE

In a semiconductor element (1) provided with a source region (3) and a drain region (4) both formed in a well (2), and a gate electrode (7) fabricated on a channel region (5), formed between these regions, through a gate insulting film (8), each element is electrically isolated by means of an SOI substrate and a field oxide film, for example, and a substrate terminal (TW) is pulled out from the channel region (5) via a contact hole formed through an inter-layer insulating film in each element at a region other than the source region (3) and drain region (4). Consequently, a 2-input-1-output element having the gate terminal (TG) and substrate terminal (TW) as two inputs can be realized, thereby making it possible to improve a packing density and operating rate while reducing the costs when forming a logic circuit or the like.

FIG. 1

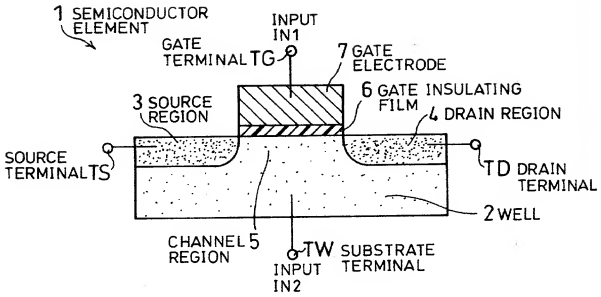

1 SEMICONDUCTOR ELEMENT
INPUT IN1
GATE TERMINAL TG
7 GATE ELECTRODE
6 GATE INSULATING FILM
3 SOURCE REGION
4 DRAIN REGION
SOURCE TERMINAL TS
TD DRAIN TERMINAL
2 WELL
CHANNEL REGION 5
TW SUBSTRATE TERMINAL
INPUT IN2

FIG. 2

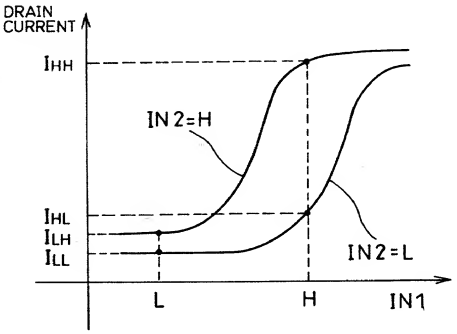

DRAIN CURRENT
IHH
IN2=H
IHL
ILH
ILL
IN2=L
L
H
IN1

FIG. 3

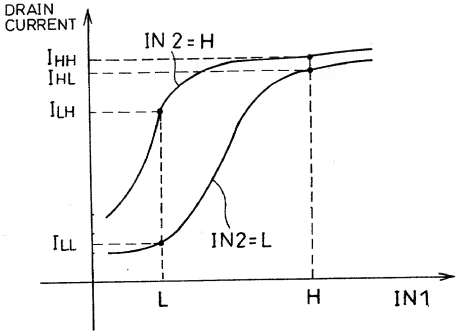

DRAIN CURRENT
IN 2 = H
IHH
IHL
ILH
ILL
IN2=L
L
H
IN1

FIG. 4

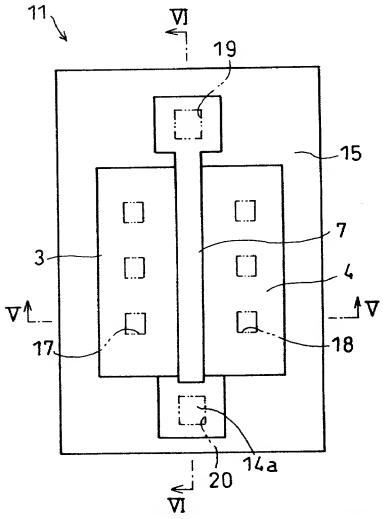

11
VI
19
15
7
3
4
V
V
17
18
14a
20
VI

FIG. 5

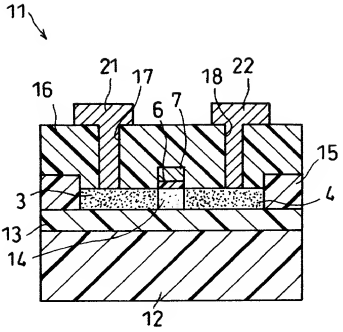


FIG. 6

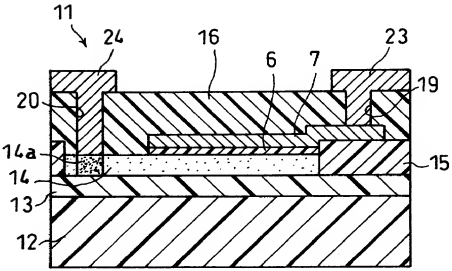


FIG. 7

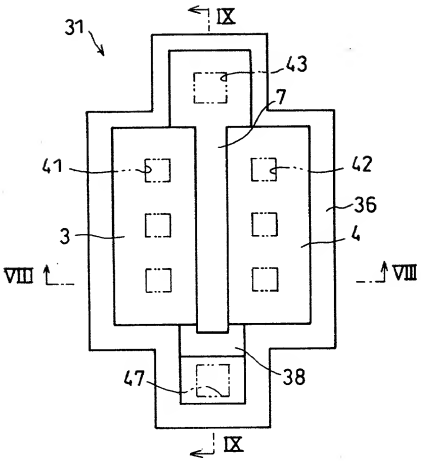

31
IX
43
7
41
42
36
3
4
VIII
VIII
47
38
IX

FIG. 8

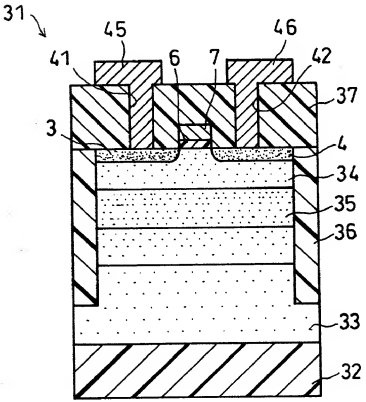

31
45
46
41
6
7
42
37
3
4
34
35
36
33
32

FIG. 9

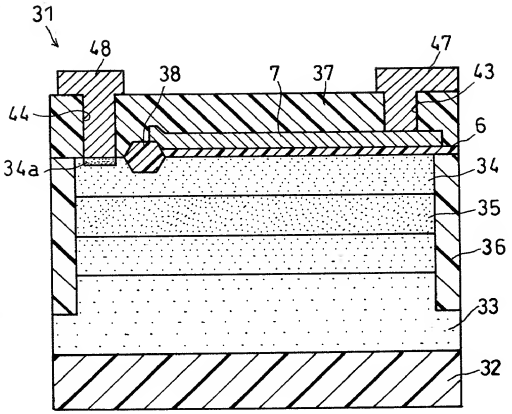
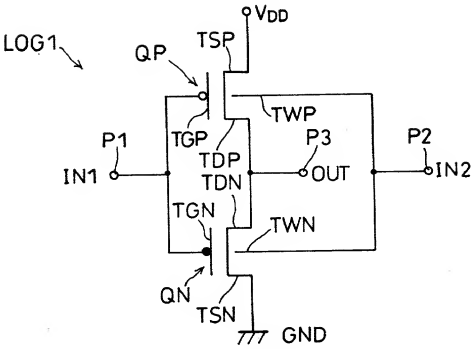


FIG.10


LOG1
QP
TSP
VDD
TWP
P1
TGP
TDP
P3
P2
IN1
TDN
OUT
IN2
TGN
TWN
QN
TSN
GND

09/424966

FIG. 11(a)

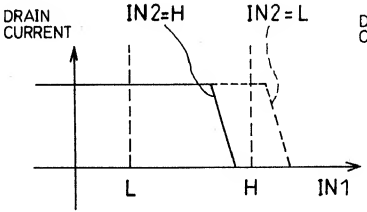


FIG. 11(b)

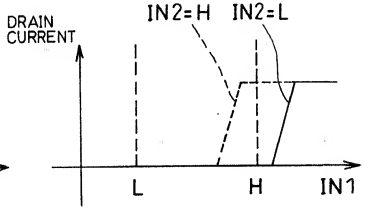


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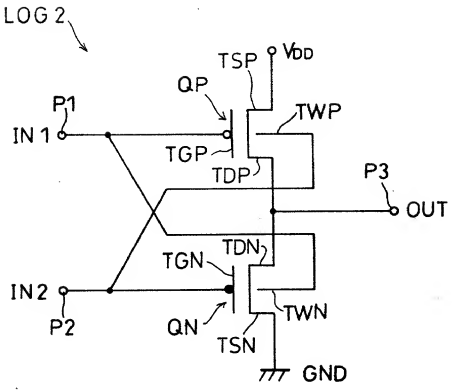
FIG. 12


LOG 2
TSP
VDD
QP
P1
TWP
IN 1
TGP
TDP
P3
OUT
TDN
TGN
IN 2
TWN
P2
QN
TSN
GND

09/424966

FIG. 13(a)

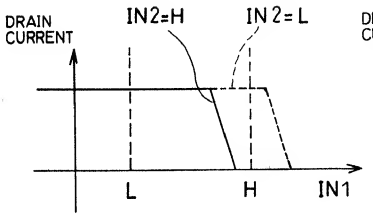


FIG. 13(b)

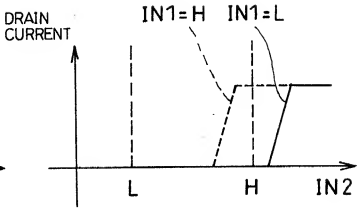


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FIG.14(a)

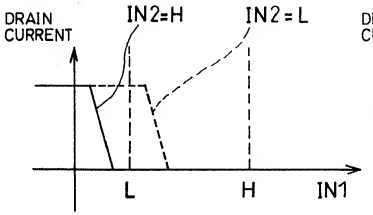

FIG.14(b)

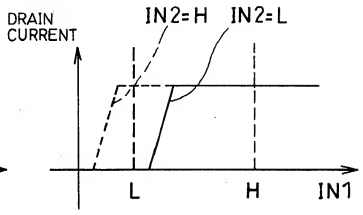

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FIG. 15(a)

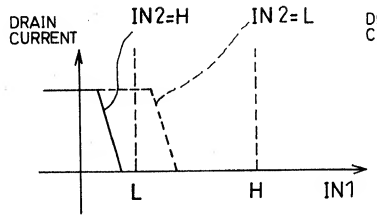

FIG. 15(b)

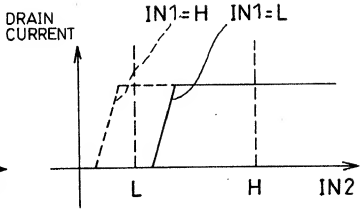

FIG. 16

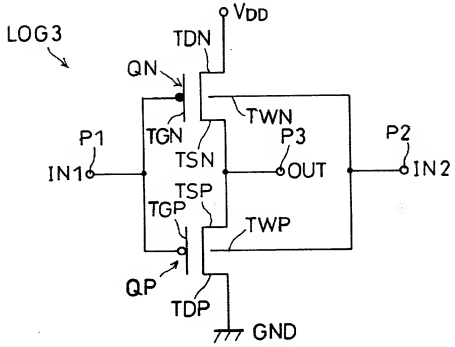
LOG3
VDD
TDN
QN
TWN
P1
TGN
P3
P2
IN1
TSN
OUT
IN2
TSP
TGP
TWP
QP
TDP
GND

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FIG.17(a)

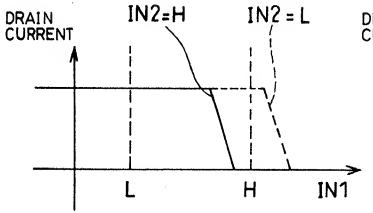

FIG.17(b)

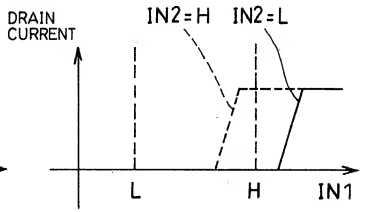

FIG. 18

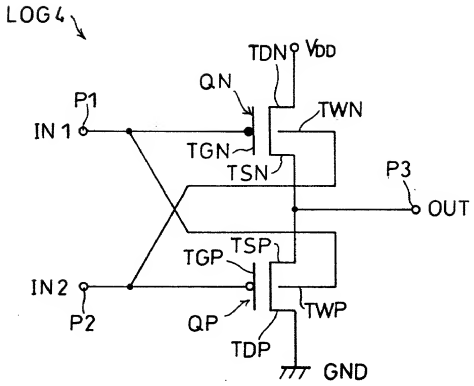
LOG4
TDN
VDD
QN
P1
TWN
IN1
TGN
TSN
P3
OUT
TSP
TGP
IN2
P2
QP
TWP
TDP
GND

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FIG.19(a)

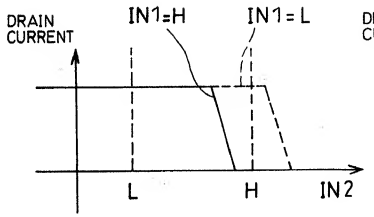

FIG.19(b)

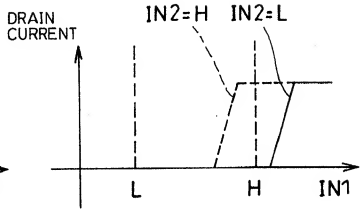

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FIG. 20(a)

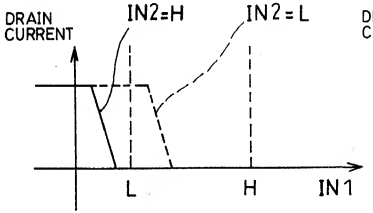

FIG. 20(b)

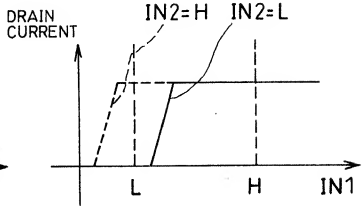

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FIG. 21(a)

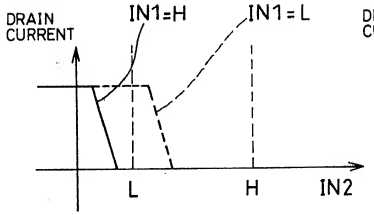


FIG. 21(b)

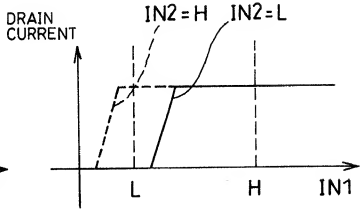


FIG. 22

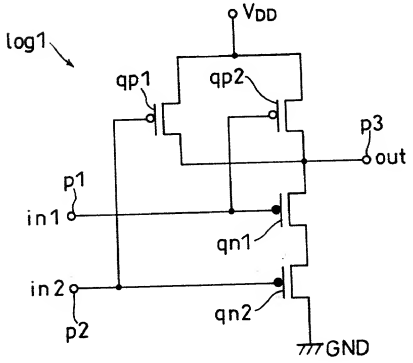
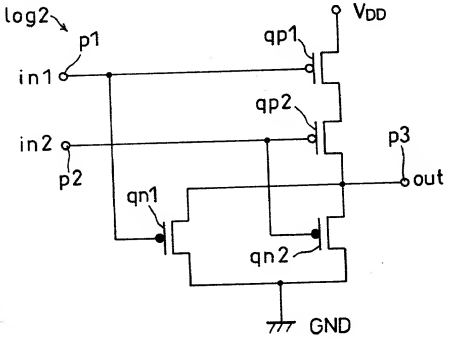


FIG. 23



DECLARATION FOR PATENT APPLICATION (Includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NUMBER 247322001700

As a below named inventor we hereby declare that:

Our residence, post office address and citizenship are as stated below next to our names,

We believewe are the original, first and joints inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR DEVICE AND DRIVING METHOD THEREOF

the specification of which (check only one item below):

☐ is attached hereto.

☒ was filed as United States application

Serial No. 09/424,966
on November 30, 1999

☒ was filed as PCT international application

Number PCT/JP98/00963
on March 9, 1998.

We hereby state that we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37 Code of Federal Regulations § 1.56(a) and (b).

We hereby claim foreign priority benefits under Title 35 United States Code § 119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119:

COUNTRY (if PCT indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. § 119
Japan	No. 9-142575	30, 05, 1997	☒ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO

Declaration for Patent Application (Continued) (Includes Reference to PCT International Applications)	ATTORNEY'S DOCKET NUMBER 247322001700

We hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120:

U.S. APPLICATIONS		STATUS *(Check one)*		
U S APPLICATION NUMBER	U S FILING DATE	PATENTED	PENDING	ABANDONED

PCT APPLICATIONS DESIGNATING THE U.S.			STATUS *(Check one)*		
PCT APPLICATION NUMBER	PCT FILING DATE	U S SERIAL NUMBERS ASSIGNED *(if any)*	PATENTED	PENDING	ABANDONED

Send correspondence to: Thomas E. Ciotti
Morrison & Foerster LLP
755 Page Mill Road
Palo Alto, California 94304-1018

Direct telephone calls to:
Thomas E. Ciotti at
(650) 813-5702

201	FULL NAME OF INVENTOR	FAMILY NAME Shibata	FIRST GIVEN NAME Akihide	SECOND GIVEN NAME	
	RESIDENCE & CITIZENSHIP	CITY Nara-shi	STATE OR FOREIGN COUNTRY Nara Japan JPX	COUNTRY OF CITIZENSHIP Japan	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS 104-B203, Misasagi-cho	CITY Nara-shi	STATE & ZIP CODE/COUNTRY Nara 631-0803 Japan	
202	FULL NAME OF INVENTOR	FAMILY NAME Iwata	FIRST GIVEN NAME Hiroshi	SECOND GIVEN NAME	
	RESIDENCE & CITIZENSHIP	CITY Ikoma-gun	STATE OR FOREIGN COUNTRY Nara Japan JPX	COUNTRY OF CITIZENSHIP Japan	
	POST OFFICE ADDRESS	POST OFFICE ADDRESS 2-4-13, Shigigaoka, Sango-cho	CITY Ikoma-gun	STATE & ZIP CODE/COUNTRY Nara 636-0813 Japan	

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 201 Akihide Shibata	SIGNATURE OF INVENTOR 202 Hiroshi Iwata	
DATE January 18, 2000	DATE January 18, 2000	

PTO/PCT Rec'd 06 MAR 2000

PATENT

Docket No. 247322001700

09/424966

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Akihide SHIBATA and Hiroshi IWATA

Serial No.: 09/424,966

Filing Date: November 30, 1999

International Application No.: PCT/JP98/00963

International Filing Date: 09 March 1998

For: SEMICONDUCTOR DEVICE AND DRIVING METHOD THEREOF

Examiner: Not Yet Assigned

Group Art Unit: Not Yet Assigned

PROSECUTION BY ASSIGNEE AND POWER OF ATTORNEY UNDER 37 C.F.R. § 3.71

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

SHARP KABUSHIKI KAISHA, the assignee of the entire right, title and interest in this patent application, under 37 C.F.R. § 3.71 hereby appoints:

Sanjay Bagade (Reg No. 42,280)
Richard R. Batt (Reg No. 43,485)
Kimberly A. Bolin (Reg No. P-44,546)
Sean Brennan (Reg No. 39,917)
Nicholas Buffinger (Reg No. 39,124)
Alan W. Cannon (Reg No. 34,977)
Robert K. Cerpa (Reg No. 39,933)
Thomas E. Ciotti (Reg No. 21,013)
Matthew M. D'Amore (Reg No. 42,457)
Stephen C. Durant (Reg No. 31,506)
Hector Gallegos (Reg No. 40,614)
Franklin Y. Han (Reg No. 41,055)
Charles D. Holland (Reg No. 35,196)
Madeline I. Johnston (Reg No. 36,174)
Erwin J. Basinski (Reg No. 34,773)
Frank P. Becking (Reg No. 42,309)
Timothy J. Bortree (Reg No. 43,506)
Barry E. Bretschneider (Reg No. 28,055)
Jingming Cai (Reg No. P-44,579)
Mark R. Carter (Reg No. 39,131)
Thomas Chuang (Reg No. P-44,616)
Steven X. Cui (Reg No. P-44,637)
Raj S. Davé (Reg No. 42,465)
Carolyn A. Favorito (Reg No. 39,183)
Kenneth R. Glick (Reg No. 28,612)
Douglas Hodder (Reg No. 41,840)
Peter Hsieh (Reg No. P-44,780)
Richard D. Jordan (Reg No. 33,519)

Ararat Kapouytian (Reg No. 40,044)
Kawai Lau (Reg No. 44,461)
Richard H. Lilley (Reg No. 42,803)
Wen Liu (Reg No. 32,822)
Harry J. Macey (Reg No. 32,818)
Thomas D. Mays (Reg No. 34,524)
Kate H. Murashige (Reg No. 29,959)
William C. Revelos (Reg No. 42,101)
Robert Saltzberg (Reg No. 36,910)
Kevin R. Spivak (Reg No. 43,148)
E. Thomas Wheelock (Reg No. 28,825)
Karen K. Wong (Reg No. 44,409)
Phanesh B. Koneru (Reg No. 40,053)
Susan K. Lehnhardt (Reg No. 33,943)
David C. Liu (Reg No. P-43,755)
David C. Lundmark (Reg No. 42,815)
Michael J. Mauriel (Reg No. 44,226)
Gladys H. Monroy (Reg No. 32,430)
Catherine M. Polizzi (Reg No. 40,130)
Paul J. Riley (Reg No. 38,596)
Debra A. Shetka (Reg No. 33,309)
Suzannah K. Sundby (Reg No. 43,172)
Thomas G. Wiseman (Reg No. 35,046)
Frank Wu (Reg No. 41,386)

all of Morrison & Foerster LLP, 755 Page Mill Road, Palo Alto, California 94304-1018, telephone (650) 813-5600, to prosecute this application and transact all matters in the United States Patent and Trademark Office connected therewith, said appointment to be to the exclusion of the inventors and their attorneys in accordance with the provisions of 37 C.F.R. § 3.71 provided that if any one of said attorneys or agents ceases being affiliated with the law firm of Morrison & Foerster as partner, employee or of counsel, such attorney's or agent's appointment as attorney or agent and all powers derived therefrom shall terminate on the date such attorney or agent ceases being so affiliated.

Please direct all written communications relative to this application to:

Thomas E. Ciotti
Morrison & Foerster LLP
755 Page Mill Road
Palo Alto, California 94304-1018

Please direct all telephone communications to Thomas E. Ciotti at (650) 813-5702.

SHARP KABUSHIKI KAISHA
a Japanese corporation

Dated: February 8, 2000

Name: Haruyasu SASAKI
Title: Group General Manager
Intellectual Property Group
Address: 22-22, Nagaike-cho, Abeno-ku
Osaka 545-8522, Japan